CCS Technical Documentation
NSB-9 Series Transceivers

System Module and User Interface

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Glossary of terms

ACI	Accessory Control Interface
ADC	Analog-Digital Converter
AEC	Acoustic Echo Canceller
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AIF	Application Interface
ALWE	Background noise suppressor
AMS	After Market Service
AMR	Adaptive Multi Rate
ARM	Processor architecture
ASIC	Application Specific Integrated Circuit
BB	Baseband
CBus	Control Bus
CCS	Customer Care Solutions
CMT	Cellular Mobile Telephone (MCU and DSP)
CPU	Central Processing Unit
CTSI	Clocking Timing Sleep Interrupt
COG	Chip On Glass
CSP	Chip Scale Package
CSTN	Color Super Twisted Nematic
DAC	Digital-Analog Converter
DAI	Digital Audio Interface
DB	Dual band

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DCN	Offset Cancellation control signal
DLL	Dynamic Link Library
DRC	Dynamic Range Controller
DSP	Digital Signal Processor
EFR	Enhanced Full Rate
EMC	Electromagnetic compatibility
EMI	Electromagnetic Interference
ESD	Electro Static Discharge
EXT RF	External RF
FBUS	Asynchronous Full Duplex Serial Bus
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
HS	Half Rate Speech
HSCSD	High Speed Circuit Switched Data
IC	Integrated Circuit
IHF	Integrated Hands Free
I/O	Input/Output
IrDA	Infrared Association
LCD	Liquid Crystal Display
LDO	Low Drop-Out
LNA	Low Noise Amplifier
MBUS	1-wire half duplex serial bus
MCU	Micro Controller Unit
MDI	MCU-DSP Interface

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MFI	Modulator and Filter Interface
PA	Transmit Power Amplifier
PC	Personal Computer
PCM	Pulse Code Modulation
PCM SIO	Synchronous serial bus for PCM audio transferring
PIFA	Planar Inverted F-antenna
PWB	Printed Wiring Board
RF	Radio Frequency
SIM	Subscriber Identity Module
UEM	Universal Energy Management
UI	User Interface
UPP	Universal Phone Processor
VCXO	Voltage Controlled Crystal Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator.

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Introduction

The system module RM9 consists of Radio Frequency (RF) and baseband (BB). User Interface (UI) contains display, keyboard, IR link, vibra, HF/HS connector and audio parts. Part of the keyboard is implemented in separate flip module, named TF9.

FM radio is located on the main PWB RM9. Headset is used as an antenna for FM radio.

The electrical part of the T9 and half of qwerty keyboard is located inside Flip. TF9 is connected to radio PWB through four 2-pole poco connectors

NSB-9 has Pop-Port™ accessory interface. Both two and three wire type of chargers are supported. BLC-2 Li-ion battery with nominal capacity of 1000 mAh is used as main power source.

The Baseband blocks provide the MCU, DSP, external memory interface and digital control functions in the UPP ASIC. Power supply circuitry, charging, audio processing and RF control hard ware are in the UEM ASIC.

The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station.

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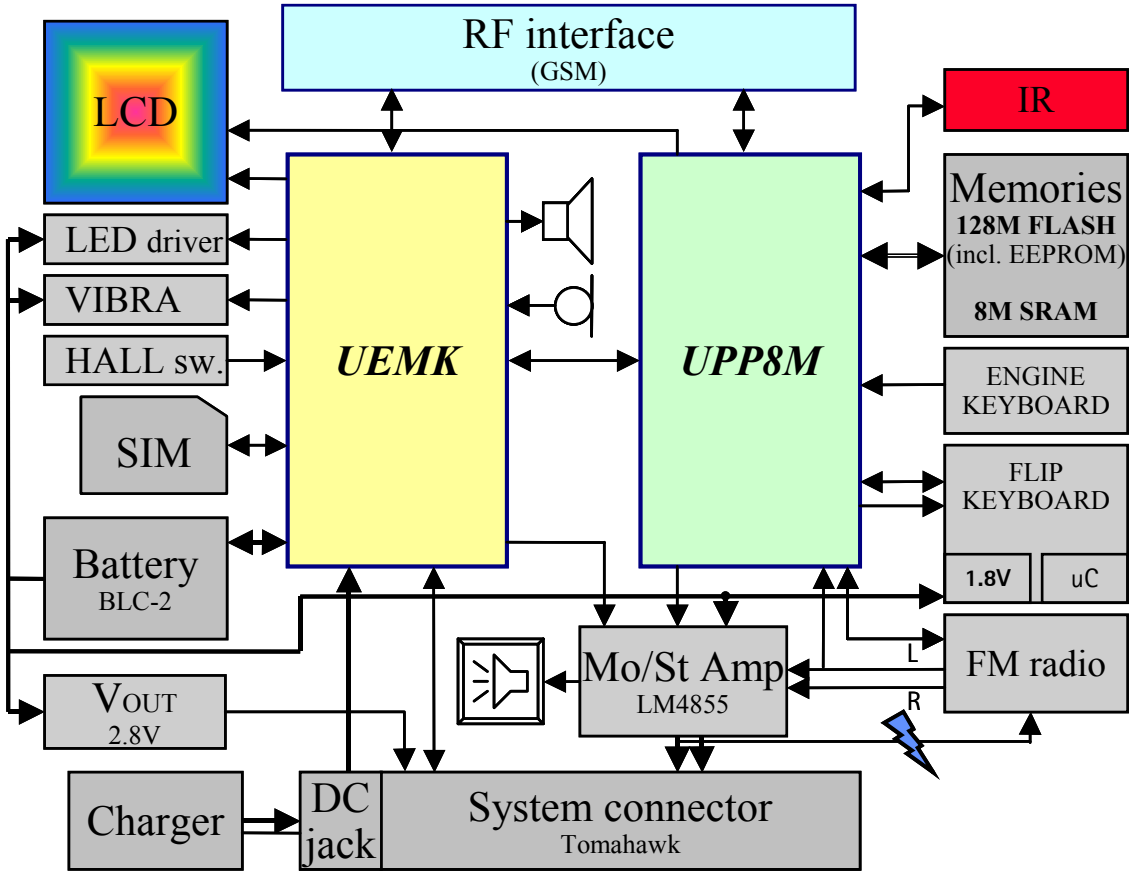
System Module: Baseband

Baseband Module, technical summary

Main functionality of the NSB-9 baseband is implemented with two ASICs: UPP (Universal Phone Processor) and UEM (Universal Energy Management).

Figure 1: Baseband Block Diagram



Baseband is running from power rails 2.8V analog voltage and 1.8V I/O voltage. UPP core voltages can be lowered down to 1.0V, 1.3V and 1.5V. UEM includes 6 linear LDO (low drop-out) regulators for baseband and 7 regulators for RF. It also includes 4 current sources for biasing purposes and internal usage. UEM also includes SIM interface which has supports both 1.8V and 3V SIM cards.

A real time clock function is integrated into the UEM which utilizes the same 32kHz clock supply as the sleep clock. A backup power supply is provided for the RTC which keeps the real time clock running when the main battery is removed. The backup power supply is a rechargeable surface mounted battery (capacitor type). The backup time with the battery is 30 minutes minimum.

The analog interface between the baseband and the RF section is handled by a UEM ASIC. UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted

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audio signals to and from the user interface. The UEM supplies the analog TXC and AFC signals to RF section according to the UPP DSP digital control. Data transmission between the UEM and the UPP is implemented using two serial busses, DBUS for DSP and CBUS for MCU. RF ASIC, Hagar, is controlled through UPP RFBUS serial interface. There is also separate signals for PDM coded audio. Digital speech processing is handled by the DSP inside UPP ASIC. UEM is a dual voltage circuit, the digital parts are running from the baseband supply 1.8V and the analog parts are running from the analog supply 2.78V also VBAT is directly used by flip, stereo amplifier, IR and some other blocks.

The baseband supports both internal and external microphone inputs and speaker outputs. UEM also includes third microphone input which is used in NSB-9 for FM radio with IHF use (Left channel). Input and output signal source selection and gain control is done by the UEM according to control messages from the UPP. Keypad tones, DTMF, and other audio tones are generated and encoded by the UPP and transmitted to the UEM for decoding. An external vibra alert control signal is generated by the UEM with separate PWM outputs.

NSB-9 has two external serial control interfaces: FBUS and MBUS. These busses can be accessed only through production test pattern.

EMC shielding for baseband is implemented using a metal shielding can. Although some components are outside the shielding can. On the other side the engine is shielded with PWB grounding. Heat generated by the circuitry will be conducted out via the PWB ground planes.

Full functionality according to the specifications needs to be met through ambient temperature range -10 °C to +55 °C. Storage temperature range -40 °C to +85 °C.

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Baseband Technical Specifications

Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Signal	Note
Battery Voltage (Idle)	-0.3V - 5.5V
Battery Voltage (Call)	Max 4.8V
Charger Input Voltage	-0.3V - 16V
Charging current	850mA

DC Characteristics

Regulators and Supply Voltage Ranges

Table 2: Battery Voltage Range

Signal	Min	Nom	Max	Note
VBAT	3.1V	3.6V	4.2V (charging high limit voltage)	3.2V SW cut off

Table 3: Baseband Regulators

Signal	Min	Nom	Max	Note
VANA	2.70V	2.78V	2.86V	I_{max} = 80mA
VFLASH1	2.70V 2.61V (Sleep)	2.78V	2.86V 2.95V (Sleep)	I_{max} = 70mA I_{sleep} = 1.5mA
VFLASH2	2.70V	2.78V	2.86V	I_{max} = 40mA
VSIM	1.745V 2.91V	1.8V 3.0V	1.855V 3.09V	I_{max} = 25mA I_{sleep} = 0.5mA
VIO	1.72V	1.8V	1.88V	I_{max} = 150mA I_{sleep} = 0.5mA
VCORE	1.0V 1.235V 1.425V 1.710V	1.053V 1.3V 1.5V 1.8V	1.106V 1.365V 1.575V 1.890V	I_{max} = 200mA I_{sleep} = 0.2mA Default value 1.5V

Table 4: Accessory Regulator

Signal	Min	Nom	Max	Note
Vout	2.72V	2.80V	2.88V	I_{max} = 80mA

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Table 5: RF Regulators

Signal	Min	Nom	Max	Note
VR1A	4.6V	4.75V	4.9V	I_{max} = 10mA
VR2	2.70V 2.61V (Sleep)	2.78V	2.86V 2.95V (Sleep)	I_{max} = 100mA
VR3	2.70V	2.78V	2.86V	I_{max} = 20mA
VR4	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR5	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR6	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR7	2.70V	2.78V	2.86V	I_{max} = 45mA

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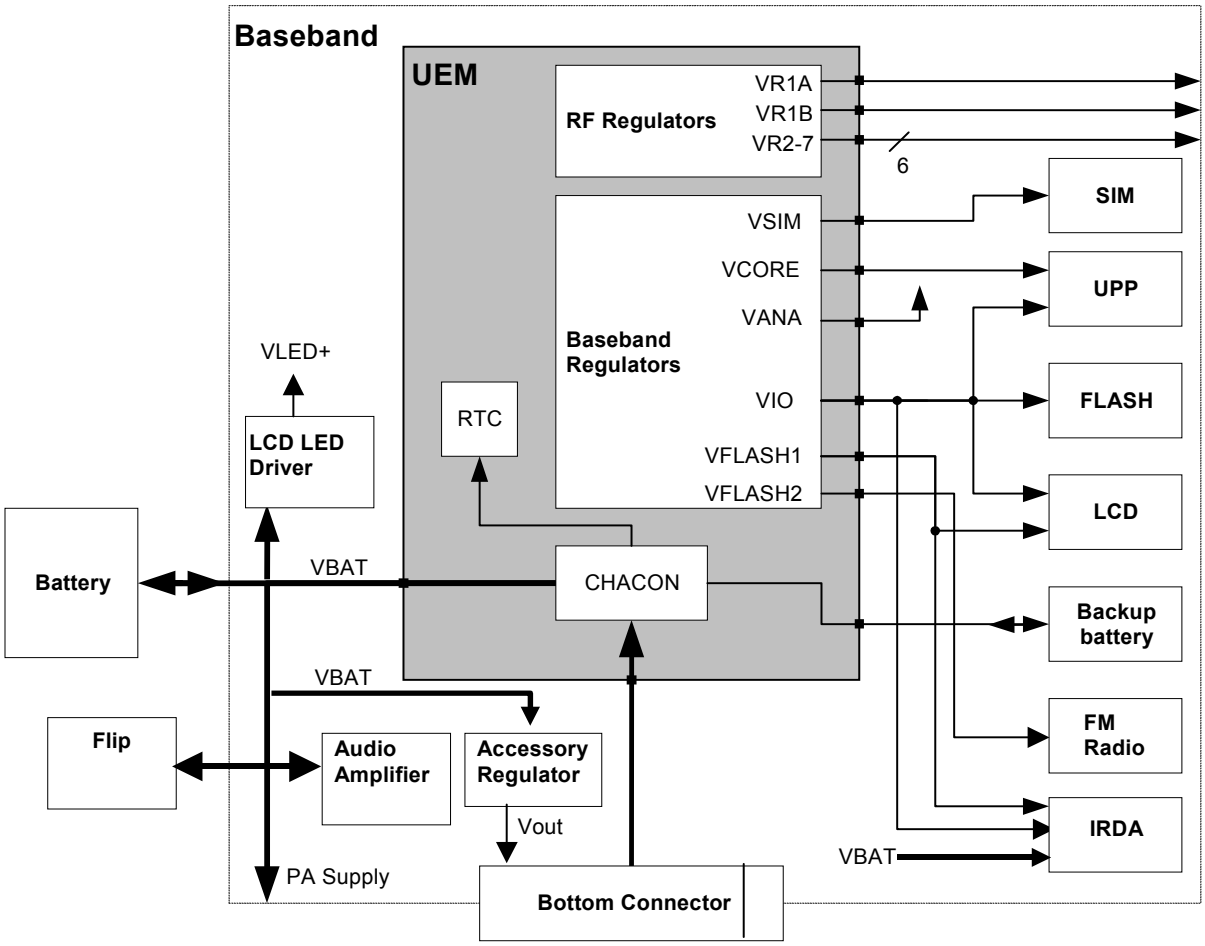
Power Distribution diagram

Figure 2: **Baseband Power Distribution Diagram**



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Baseband External and Internal Signals and Connections

This section describes the external and internal electrical connection and interface levels on the baseband. Electrical interface specifications are collected into tables that covers a connector or a defined interface.

Internal Signals and Connections

Table 6: FM Radio Interface

BB Signal	FM Radio Signal	Min	Nom	Max	Condition	Note
VFLASH2	VCC	2.7V	2.78 V	2.86V		Analog supply voltage
		6.0mA	8.4mA	10.5mA	Operational	
			3uA	6uA	Stand by	
	VDIG	2.7V	2.78V	2.86V		Digital supply voltage
		2.1mA	3.0mA	3.9mA	Operational	
		11uA	19uA	26uA	Stand by (bus enable LOW)	
GenIO(3)	FMClk	1.4V 0	1.8V	1.88V 0.4V	High Low	Reference clock for FM radio module Also 6.5MHz or 13MHz can be used
			32kHz		Frequency	
GenIO(8)	FMWrEn	1.4V 0V	1.8V	1.88V 0.4V	High Low	Write Enable
GenIO(11)	FMCtrlClk	1.4V 0	1.8V	1.88V 0.4V	High Low	max. 1MHz
GenIO(12)	FMCtrlDa	1.4V 0	1.8V	1.88V 0.4V	High Low	Bidirectional
FMANT	$f_{FM(ant)}$	76MHz		108MHz		FM input frequency. Headset used as an antenna.
FM_RADIO R	VAFR	720mV	850mV	940mV	f_{RF}=98MHz, V_{RF}=1mV	FM-radio output signal (right) to amplifier input
FM_RADIO L	VAFL	720mV	850mV	940mV	f_{RF}=98MHz, V_{RF}=1mV	FM-radio output signal (left) to amplifier input

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Table 7: AC and DC Characteristics of RF-Baseband Voltage Supplies

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VBAT	Battery	PA, UEM, STEREO AMPLI-FIER, FLIP	Voltage	2.95	3.6	4.2	V	Battery supply.
			Current			3	A	
			Current drawn by PA when "off"		0.8	2	uA	
VR1A	UEM	VCP	Voltage	4.6	4.75	4.9	V	Supply for varactor for UHF VCO tuning.
			Current		2	10	mA	
VR2	UEM	VRF_TX	Voltage	2.70	2.78	2.86	V	Supply for part of transmit strip. Supply for TX I/Q-modulators.
			Current		65	100	mA	
VR3	UEM	VCTCXO	Voltage	2.70	2.78	2.86	V	Supply for VCTCXO
			Current		1	20	mA	
VR4	UEM	VRF_RX	Voltage	2.70	2.78	2.86	V	Supply for Hagar RX; preamp., mixer,DTOS Noise density decades 20dB/dec from 6Hz to 600Hz. From f >600Hz maximum noise density 55nV$_{RMS}$/ÖHz.
			Current			50	mA	
VR5	UEM	VDIG, VPRE, VLO	Voltage	2.70	2.78	2.86	V	Supply for Hagar PLL; dividers, LO-buffers, prescaler.
			Current			50	mA	
VR6	UEM	VBB	Voltage	2.70	2.78	2.86	V	Supply for Hagar BB and LNA
			Current			50	mA	
VR7	UEM	UHF VCO	Voltage	2.70	2.78	2.86	V	Supply for UHF VCO
			Current			30	mA	

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VrefRF01	UEM	VREF_RX	Voltage	1.334	1.35	1.366	V	Voltage Reference for RF-IC. Note:Below 600Hz noise density is allowed to increase 20 dB/oct
			Current			100	uA	
VrefRF02	UEM	VB_EXT	Voltage	1.323	1.35	1.377	V	Supply for RF-BB digital interface and some digital parts of RF.
			Current			100	uA	

Table 8: AC and DC Characteristics of RF-Baseband Digital Signals

Signal name	From	To	Parameter	Input Characteristics				Function
				Min	Typ	Max	Unit	
TXP (RFGenOut3)	**UPP**	**PA & HAGAR**	**"1"**	**1.38**		**1.88**	**V**	**Transmitter power amplifier enable / DCN2 timing???**
			"0"	**0**		**0.4**	**V**	
			Load Resistance	**10**		**220**	**kohm**	
			Load Capacitance			**20**	**pF**	
			Timing Accuracy			**1/4**	**symbol**	
RFBusEna1X	**UPP**	**HAGAR**	**"1"**	**1.38**		**1.88**	**V**	**RFbus enable**
			"0"	**0**		**0.4**	**V**	
			Current			**50**	**uA**	
			Load resistance	**10**		**220**	**kohm**	
			Load capacitance			20	pF	
RFBusData	UPP	HAGAR	"1"	1.38		1.88	V	RFbus data; read/write
			"0"	0		0.4	V	
			Load resistance	10		220	kohm	
			Load capacitance			20	pF	

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			Data frequency			10	MHz	
RFBusClk	UPP	HAGAR	"1"	1.38		1.88	V	RFbus clock
			"0"	0		0.4	V	
			Load resistance	10		220	kohm	
			Load capacitance			20	pF	
			Data frequency			10	MHz	
RESET (GenI/O6)	UPP	HAGAR	"1"	1.38		1.85	V	Reset to Hagar
			"0"	0		0.4	V	
			Load capacitance			20	pF	
			Load resistance	10		220	kohm	
			Timing accuracy			1/4	sym-bol	

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Table 9: AC and DC Characteristics of RF-Baseband Analogue Signals

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VCTCXO	**VCTCXO**	**UPP**	**Frequency**	**13**		**26**	**MHz**	**High stability clock signal for the logic circuits, AC coupled. Distorted sinewave eg. sawtooth.**
			Signal amplitude	**0.2**	**0.8**	**2.0**	**Vpp**	
			Input Impedance	**10**			**kohm**	
			Input Capacitance			**10**	**pF**	
			Duty Cycle	**40**		**60**	**%**	
VCTCXOGnd	VCTXO	UPP	DC Level		0		V	Ground for reference clock
RXI/RXQ	HAGAR	UEM	Differential voltage swing (static)	1.35	1.4	1.45	Vpp	RX baseband signal.
			DC level	1.3	1.35	1.4	V	
TXIP / TXIN	UEM	HAGAR	Differential voltage swing (static)	2.23		2.48	Vpp	Programmable voltage swing. Programmable common mode voltage. Between TXIP-TXIN
			DC level	1.17	1.20	1.23	V	
			Source Impedance			200	ohm	
TXQP / TXQN	UEM	HAGAR	Same spec as for TXIP / TXIN					Differential quadrature phase TX baseband signal for the RF modulator
AFC	UEM	VCTCXO	Voltage Min Max	0.0 2.4		0.1 2.6	V	Automatic frequency control signal for VCTCXO
			Resolution	11			bits	
			Load resistance and capacitance	1		100	kohm nF	

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			Step settling time			0.2	ms	
Aux_DAC (TxC)	UEM	RF	Voltage Min Max	2.4		0.1	V	Transmitter power control
			Source Imped-ance			200	ohm	
			Resolution	10			bits	
RFTemp	RF	UEM	Voltage at -20°C		1,57		V	Temperature sensor of RF.
			Voltage at +25°C		1,7			
			Voltage at +60°C		1,79			
Vbase	RF	UEM	Voltage			2.7	V	Detected voltage from PA power level sensing unit

Table 10: Engine keyboard interface

UPP Pin	Signal	Min	Nom	Max	Condition	Note
P00	COL(0)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix column 0
P01	COL(1)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix column 1
P02	COL(2)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix column 2
P03	COL(3)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix column 3
P04	COL(4)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix column 4
P05 / GenI/O2	COL(5)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix column 5
P10	ROW(0)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix row 0
P11	ROW(1)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix row 1
P12	ROW(2)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix row 2
P13	ROW(3)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix row 3
P14	ROW(4)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix row 4

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P15	ROW(5)	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Keyboard matrix row 5
GenI/O19	Shift	0.7xVIO 0	1.8V	VIO 0.3xVIO	High Low	Engine shift key

Table 11: Stereo ampilifer interface

BB signal	Stereo amplifier signal	Min	Nom	Max	Condition	Note
VBAT	Vcc	3.1V	3.6V	4.2V		Supply voltage
			7.5mA	10mA	Output mode 7, Vin=0V, Io=0A	
			0.5uA		Standby	
GND	GND		0V			Ground
GenI/O14	ENB	1.4V 0V	1.8V	1.88V 0.4V	High Low	Chip enable, active high
GenI/O15	CLK	1.4V 0V	1.8V	1.88V 0.4V	High Low	Clock input
GenI/O16	DATA	1.4V 0V	1.8V	1.88V 0.4V	High Low	Serial data input
FM-RADIO L, FM-RADIO R	Lin, Rin	GND		Vcc		Lin, Rin input voltage
XEAR	Phone InHS, Phone InIHF	GND		Vcc		Phone in input voltage

External Signals and Connections

Table 12: Flip Connectors

Pin / Ref	Signal	Min	Nom	Max	Condition	Note
J301 J302	VBAT	3.1V	3.6 V	4.2V	Flip Closed	Flip supply voltage
		2.9V	3.4V	4.0V	Flip Open, (load switch)	
J303, J304	DATA	0.7xVIO 0		0.3xVIO	High Low	GenI/O17
J305, J306	CLOCK	0.7xVIO 0		0.3xVIO	High Low	GenI/O18
J307, J308	GND		0V			Ground

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Table 13: LCD Connector (X300)

Pin	Signal	Min	Nom	Max	Condition	Note
1	VDD (VFLASH1)	2.72V	2.78V	2.86V		Voltage supply Connected to VFLASH1
2	XRES	0.8xVIO 0		VIO 0.22xVIO	Logic '1' Logic '0'	Reset Active low
		1000ns			t_{rw}	Reset active
3	SI	0.8xVIO 0		VIO 0.22xVIO	Logic '1' Logic '0'	Serial data (driver input)
		100ns			t_{sds}	Data setup time
		100ns			t_{sdh}	Data hold time
4	VDDI (VIO)	1.72V	1.8V	1.88V		Logic voltage supply Connected to VIO
5	XCS	0.8xVIO 0		VIO 0.22xVIO	Logic '1' Logic '0'	Chip select Active low
		130ns			t_{css}	XCS low before SCLK rising edge
		130ns			t_{csh}	XCS low after SCLK rising edge
		300ns			t_{csw}	XCS high pulse width
6	SCLK	0.8xVIO 0		VIO 0.22xVIO 6.5MHz	Logic '1' Logic '0' Max frequency	Serial clock input
		250ns			t_{scyc}	Clock cycle
		110ns			t_{shw}	Clock high
		110ns			t_{slw}	Clock low
7	GND		0V			Ground
8	LED -	 0.505V	0V 0.525V	 0.545V	LEDs OFF LEDs ON	
9	NC					Not connected
10	LED +	9.505V (9V+LED-)	0V 11.325V (10.8V+LED-)	12.545V (12V+LED-)	LEDs OFF LEDs ON	Supply voltage for LCD LEDs

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Table 14: DC Connector (X101)

Pin	Signal	Min	Nom	Max	Condition	Note
1	VCHAR		11.1V_{peak}	16.9 V_{peak} 7.9 V_{RMS} 1.0 A_{peak}	Standard charger	Charger positive input
		7.0 V_{RMS}	8.4 V_{RMS}	9.2 V_{RMS} 850 mA	Fast charger	
2	CHGND		0			Charger ground

Table 15: System Connector (X102)

Pin	Signal	Description	Spectral range	UI levels	Impedance	Note
1	CHARGE	Charge Voltage	DC	0...9V 0.85A		
2	GND	Charge GND			100mΩ (PWB + connector)	
3	ACI	Accessory Control Interface	1 kbit/s	0V 2.78V	47Ω	Insertion & removal / Control
4	VOUT	DC out	DC	2.78V 70mA	100mΩ (PWB + connector)	
5						Not connected in NSB-9
6	FBUS RX		115 kbit/s	0...0.86V (logic "0") 2.0...3.0V (logic "1")	33Ω	
7	FBUS TX		115 kbit/s	0...0.81V (logic "0") 1.89...2.83 V (logic "1")	33Ω	
8						Not connected in NSB-9
9	XMIC N	External mic input	300...8k			
10	XMIC P	External mic input	300...8k	2.1V DC		
11	HSEAR N	Ext audio output (left)	20...20k		10Ω	Differential left channel output

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12	HSEAR P	Ext audio ouput (left)	20...20k		10Ω	
13	HSEAR R N	Ext audio output (right)	20...20k		10Ω	Differential right channel output
14	HSEAR R P	Ext audio output (right)	20...20k		10Ω	

Table 16: SIM Connector (X386)

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	VSIM	1.8V SIM Card	1.6	1.8	1.9	V	Supply voltage
		3V SIM Card	2.8	3.0	3.2		
2	SIMRST	1.8V SIM Card	0.9xVSIM 0		VSIM 0.15xVSIM	V	SIM reset (output)
		3V SIM Card	0.9xVSIM 0		VSIM 0.15xVSIM		
3	SIMCLK	Frequency		3.25		MHz	SIM clock
		Trise/Tfall			50	ns	
		1.8V Voh 1.8V Vol	0.9xVSIM 0		VSIM	V	
		3 Voh 3 Vol	0.9xVSIM 0		VSIM		
4	DATA	1.8V Voh 1.8V Vol	0.9xVSIM 0		VSIM 0.15xVSIM	V	SIM data (output)
		3 Voh 3 Vol	0.9xVSIM 0		VSIM 0.15xVSIM		
		1.8V Vih 1.8V Vil	0.7xVSIM 0		VSIM 0.15xVSIM		SIM data (input) Trise/Tfall max 1us
		3V Vil 3V Vil	0.7xVSIM 0		VSIM 0.15xVSIM		
5	NC						Not Connected
6	GND	GND		0		V	Ground

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Table 17: Internal Microphone

Signal	Min	Nom	Max	Condition	Note
MICP			200mV_{pp}	AC	2.2kΩ to MIC1B
	2.0 V	2.1 V	2.25 V	DC	
MICN	2.0V	2.1V	2.25V	DC	

Table 18: Internal Speaker

Signal	Min	Nom	Max	Condition	Note
EARP	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	Differential output (V_{diff} = 4.0 V_{pp})
EARN	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	

Table 19: Integrated hands free speaker

Signal	Min	Nom	Max	Condition	Note
IHFP	V	V	V_{pp} V	AC DC	Differential output Vbat 4.1V, 1kHz, 8Ω, 1% THD (V_{diff} = 2.4V_{pp})
IHFN	V	V	V_{pp} V	AC DC	

Table 20: Internal vibra

Signal	Min	Nom	Max	Condition	Note
VBAT	3.1V	3.6V	4.2V		
VIBRA	1.0V	1.5V	2.3V	DC	Udc_motor

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Baseband Functional Description

Modes of Operation

NSB-9 baseband has six different functional modes:

- No supply
- Back-up
- Acting Dead
- Active
- Sleep
- Charging

No supply

In NO_SUPPLY mode the phone has no supply voltage. This mode is due to disconnection of main battery and backup battery or low battery voltage level in both of the batteries.

Phone is exiting from NO_SUPPLY mode when sufficient battery voltage level is detected. Battery voltage can rise either by connecting a new battery with VBAT > VMSTR+ or by connecting charger and charging the battery above VMSTR+.

Backup

In BACKUP mode the backup battery has sufficient charge but the main battery can be disconnected or empty (VBAT < VMSTR and VBACK > VBUCOFF).

VRTC regulator is disabled in BACKUP mode. VRTC output is supplied without regulation from backup battery (VBACK). All the other regulators are disabled.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called "Acting Dead". To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

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One of the sub-state of the active mode is FM radio on state. In that case UEM audio blocks, stereo amplifier and FM radio are powered on. FM radio circuitry is controlled by the MCU and 32kHz reference clock is supplied by the UPP. VFLASH2 regulator is operating.

In active mode the RF regulators are controlled by SW writing into UEM's registers wanted settings: VR1A can be enabled or disabled. VR2 can be enabled or disabled and its output voltage can be programmed to be 2.78V or 3.3V. VR4 - VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode.

Sleep mode

Sleep mode is entered when both MCU and DSP are in stand-by mode. Sleep is controlled by both processors. When SLEEPX low signal is detected UEM enters SLEEP mode. VCORE, VIO and VFLASH1 regulators are put into low quiescent current mode. All RF regulators are disabled in SLEEP. When SLEEPX=1 is detected UEM enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection etc.

In sleep mode VCTCXO is shut down and 32 kHz sleep clock oscillator is used as reference clock for the baseband.

Charging

Charging can be performed in any operating mode. The battery type/size is indicated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

The battery voltage, temperature, size and current are measured by the UEM controlled by the charging software running in the UPP. Only Li-ion batteries are charged by NSB-9.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEM switch off when the battery voltage has reached 4.2 V. Charging current is monitored by measuring the voltage drop across a 220 mΩ precision resistor.

Power Up and Reset

Power up and reset is controlled by the UEM ASIC. NSB-9 baseband can be powered up in following ways:

1 Press power button which means grounding the PWRONX pin of the UEM

2 Connect the charger to the charger input

3 Supply battery voltage to the battery pin

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4 RTC Alarm, the RTC has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20ms delay and then enters it's reset mode. The watchdog starts up, and if the battery voltage is greater than Vcoff+ a 200ms delay is started to allow references etc. to settle. After this delay elapses the VFLASH1 regulator is enabled. 500us later VR3, VANA, VIO and VCORE are enabled. Finally the PURX (Power Up Reset) line is held low for 20 ms. This reset, PURX, is fed to the baseband ASIC UPP, resets are generated for the MCU and the DSP. During this reset phase the UEM forces the VCTCXO regulator on regardless of the status of the sleep control input signal to the UEM. The FLSRSTx from the ASIC is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on at the UEM power on except VSIM and VFLASH2 regulators which are controlled by the MCU. The UEM internal watchdogs are running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires the UEM returns to power off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

Power up with PWR key

When the Power on key is pressed the UEM enters the power up sequence as described above. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notice that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stay low for a certain time the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key do not indicate a valid power on situation the MCU powers off the baseband.

Power up when charger is connected

In order to be able to detect and start charging in a case where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY or BACKUP mode of UEM) charging is controlled by START-UP CHARGING circuitry.

Whenever VBAT level is detected to be below master reset threshold (VMSTR-) charging is controlled by START_UP charge circuitry. Connecting a charger forces VCHAR input to rise above charger detection threshold, VCHDET+. By detection start-up charging is started. UEM generates 100mA constant output current from the connected charger's output voltage. As battery charges its voltage rises, and when VBAT voltage level higher than master reset threshold limit (VMSTR+) is detected START_UP charge is terminated.

Monitoring the VBAT voltage level is done by charge control block (CHACON). MSTRX='1' output reset signal (internal to UEM) is given to UEM's RESET block when VBAT>VMSTR+ and UEM enters into reset sequence described earlier.

If VBAT is detected to fall below VMSTR- during start-up charging, charging is cancelled. It will restart if new rising edge on VCHAR input is detected (VCHAR rising above VCHDET+).

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Power up when battery is connected

Baseband can be powered up by connecting battery with sufficient voltage. Battery voltage has to be over UEM internal comparator threshold level, Vcoff+. Battery low limit is specified in Table 2. When proper battery voltage is detected UEM enters to reset sequence as described earlier.

RTC alarm power up

If phone is in POWER_OFF mode when RTC alarm occurs the wake up procedure is as described in section 5.5. After baseband is powered on an interrupt is given to MCU. When RTC alarm occurs during ACTIVE mode the interrupt for MCU is generated.

A/D Channels

The UEM contains the following A/D converter channels that are used for several measurement purposes. The general slow A/D converter is a 10 bit converter using the the UEM interface clock for the conversion. An interrupt will be given at the end of the measurement.

The UEM's 11-channel analog to digital converter is used to monitor charging functions, battery functions, voltage levels in external accessory detection inputs, user interface and RF functions.

The monitored battery functions are battery voltage (VBATADC), battery type (BSI) and battery temperature (BTEMP) indication.

The battery type is recognized through a resistive voltage divider. In phone there is a 100kOhm pull up resistor in the BSI line and the battery has a pull down resistor in the same line. Depending on the battery type the pull down resistor value is changed. The battery temperature is measured equivalently except that the battery has a NTC pull down resistor in the BTEMP line.

KEYB1&t2 inputs are used for keyboard scanning purposes. These inputs are also routed internally to the miscellaneous block. In NSB-9 KEYB1 input is used for flip position detection.

The HEADINT and HOOKINT are external accessory detection inputs used for monitoring voltage levels in these inputs. They are routed internally from the miscellaneous block and they are connected to the converter through a 2/1 multiplexer. HOOKINT is not used in NSB-9. HEADINT is connected to System Connector ACI line, and it is switched inside the UEM to MBUS line.

The monitored RF functions are PATEMP and VCXOTEMP detection. PATEMP input is used to measure temperature of the HAGAR RFIC. VCXOTEMP is not used in NSB-9.

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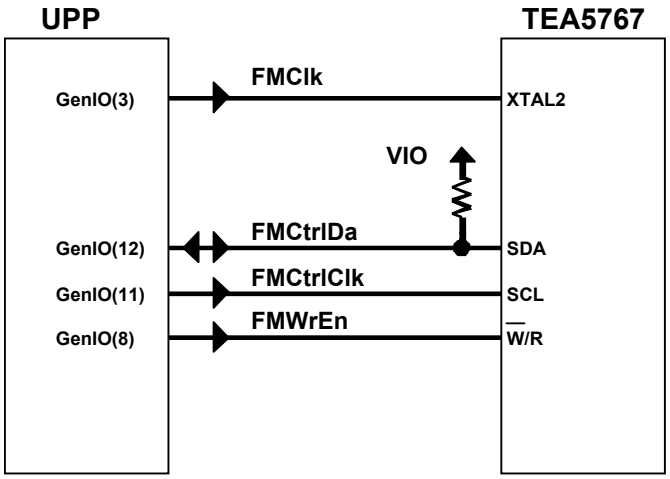
FM Radio

FM radio circuitry used in NSB-9 is a single-chip electronically tuned FM stereo radio with fully integrated IF selectivity and demodulation. The radio is completely adjustment-free and does only require a minimum of small and low cost external components. It has signal dependent mono/stereo blend [Stereo Noise Cancelling (SNC)]. The radio can tune the European, US and Japan FM bands.

FM-radio digital interface 3-wire bus contains write/read, clock and data lines. The bus operates at maximum clock frequency of 1MHz. Channel tuning and other controls are controlled through serial bus interface by the MCUSW. Reference clock, 32kHz, is generated by the UPP CTSI block (32kHz from sleep clock)

Figure 3: FM radio digital interface.



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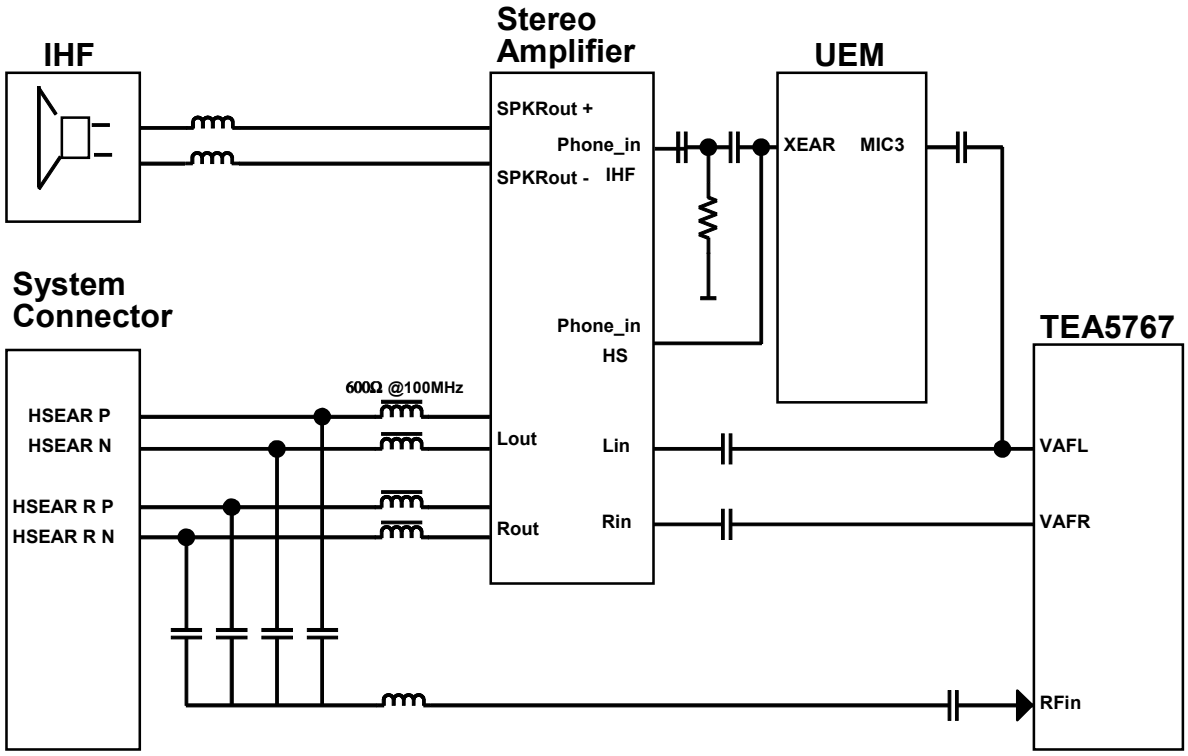
FM-radio audio connections

FM-radio audio output signals are fed to stereo audio amplifier Rin and Lin inputs and UEM microphone input MIC3. Amplification of the audio signal is made by the audio circuitry inside the UEM (IHF mode) and stereo audio amplifier. In IHF mode the left audio signal is looped internally in UEM from MIC input to XEAR output, which is connected to stereo audio amplifier Phone input (Phone InHS and Phone InIHF). Amplified audio signal is fed to IHF speaker or headset, which is also used as an antenna input for the radio. FM radio audio output is muted during the search operation.

Figure 4: FM radio audio and antenna connections



Keyboards

NSB-9 keyboard consists of engine keyboard and separate FLIP keyboard. Flip module is connected to main PWB through 4pcs 2-pole pogo pin connectors. Flip position detection is implemented with HALL sensor switch. The switch is connected to UEM KEYB1 A/D channel. Magnet is located inside the flip. According to the position detection, parts of flip keyboards are enabled/disabled.

Engine Keyboard

6x6 matrix keyboard is used in engine side. Key pressing is detected by scanning procedure. Keypad signals are connected UPP keyboard interface. Side keys are included to matrix. Engine shift key is connected to UPP GenI/O19. Power key is working as the third SW key when flip is open.

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Table 21: Power key function

Flip position	Power key	Note
Closed	Power key	
Open	3rd SW key	Right SW key is working as power key.

When no key is pressed row inputs are high due to UPP internal pull-up resistors. The columns are written zero. When key is pressed one row is pulled down and an interrupt is generated to MCU. After receiving interrupt MCU starts scanning procedure. All columns are first written high and then one column at the time is written down. All other columns except one which was written down are set as inputs. Rows are read while column at the time is written down. If some row is down it indicates that key which is at the cross point of selected column and row was pressed. After detecting pressed key all register inside the UPP are reset and columns are written back to zero.

Table 22: Engine keyboard matrix

	P10	P11	P12	P13	P15	P15
P00	6	7	8	9	0	Backspace
P01	Y	U	I	O	P	=
P02	H	J	K	L	;	'
P03	N	M	,	.	/	ENTER
P04	SW right	END	Arrow up	Arrow left	Arrow right	Arrow down
P05	SW left	SEND	Space	Vol up	Vol down	

GenI/O 19	Shift

Flip

Part of the NSB-9 keyboard is implemented in a separate flip module, which is double sided. Top side consists of so called ITU-T keys (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, * and #). On the other side (inner side) there is a half of so called qwerty keys.

There are 4 contacts (2 in parallel) from engine to flip: Supply voltage, grounding, clock and data lines. VBAT is used as flip power supply. There is a 1.8V / 50mA regulator inside the flip for uController power supply. Upper VBAT voltage for flip is disabled with load switch when flip is closed. When the flip is open, the lower VBAT voltage for the flip is disabled with another loadswitch (U320)

Flip keyboard

4x9 matrix is used in flip keyboard. The matrix is connected to flip MCU. Character and shift keys are connected to own inputs to enable simultaneus key pressings. Matrix key pressing is detected with scanning. Character and shift keypressings are detected by I/O port interrupts. Flip MCU is connected to the engine with serial data and clock lines (UPP GenI/O17 and 18).

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Flip position detection

Flip position detection is implemented with HALL sensor switch (TLE4917) and magnet. HALL switchs is located in engine top side, and magnet is inside the flip mechanics. HALL switch output is connected to UEM KEYB1 AD input. Trigger level is 2.27V(min), 2.5V(typ), 2.69V(max) with 15...40mV hysteresis. HALL switch senses the possible presence of a magnet located inside the flip. Sensing is done by polling, the device wakes up every 140ms and stays awake about 50us. When the flip is closed the output sensor is floating , and an external 100k pull-up resistor is sets the line to 2.78V. Opening the flip will move the magnet away from the sensing distance, and sensor output is driven down.

IR Module

The IR interface, when using 1.8V transceiver, is designed into the UPP. The IR link supports speeds from 9600 bit/s to 1.152 MBit/s up to distance of 80cm (2 feet 7 inches). Transmission over the IR if half-duplex.

IR transceiver can be set into shut-down mode by setting SD pin to logic '1' for low current consumption. Shut-down mode is used all the time when IR transceiver is not in use.

SIM Interface

UEM contains the SIM interface logic level shifting. SIM interface can be programmed to support 3V and 1.8V SIMs. SIM supply voltage is selected by a register in the UEM. It is only allowed to change the SIM supply voltage when the SIM IF is powered down.

The SIM power up/down sequence is generated in the UEM. This means that the UEM generates the RST signal to the SIM. Also the SIMCardDet signal is connected to UEM. The card detection is taken from the BSI signal, which detects the removal of the battery. The monitoring of the BSI signal is done by a comparator inside UEM. The SIM interface is powered up when the SIMCardDet signal indicates "card in". This signal is derived from the BSI signal.

Table 23: SIMCARDet Detection

Parameter	Variable	Min	Typ	Max	Unit
SIMCARDet, BSI comparator Threshold	**Vkey**	**1.94**	**2.1**	**2.26**	**V**
SIMCardDet, BSI comparator Hysteresis (1)	**Vsimhyst**	**50**	**75**	**100**	**mV**

The whole SIM interface locates in two chips: UPP and UEM.

The SIM interface in the UEM contains power up/down, port gating, card detect, data receiving, ATR-counter, registers and level shifting buffers logic. The SIM interface is the electrical interface between the Subscriber Identity Module Card (SIM Card) and mobile phone (via UEM).

The data communication between the card and the phone is asynchronous half duplex. The clock supplied to the card is in GSM system 1.083 MHz or 3.25 MHz.

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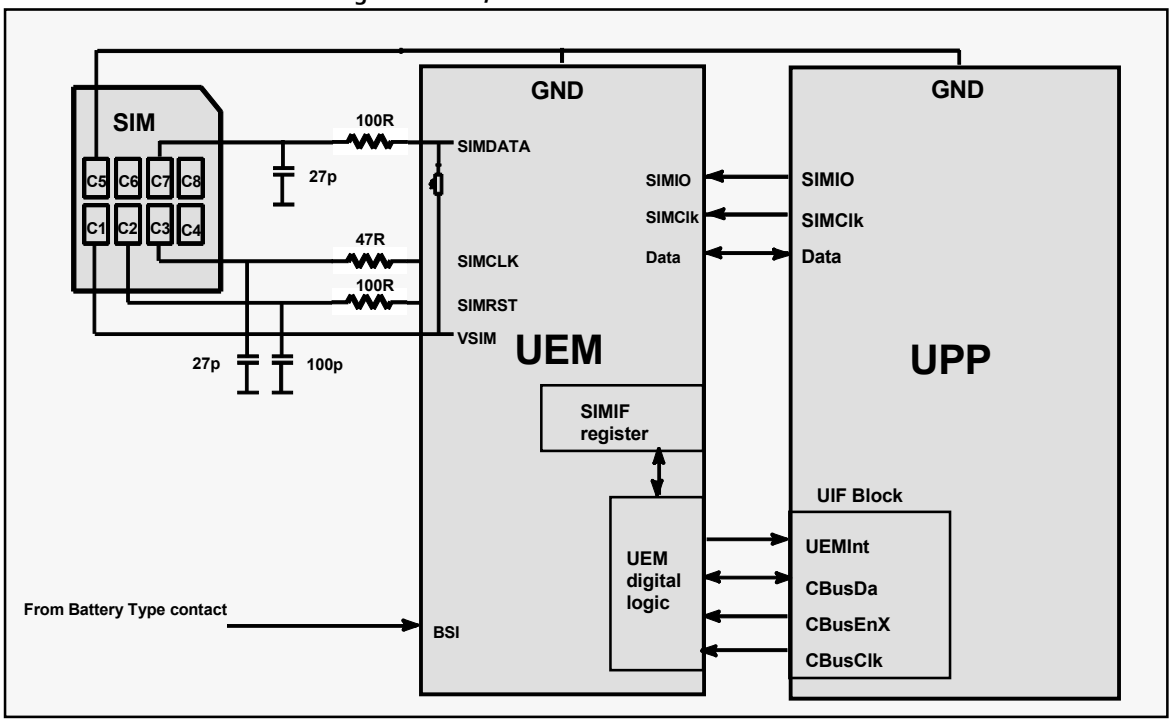
Figure 5: UPP/UEM SIM Interface Connections



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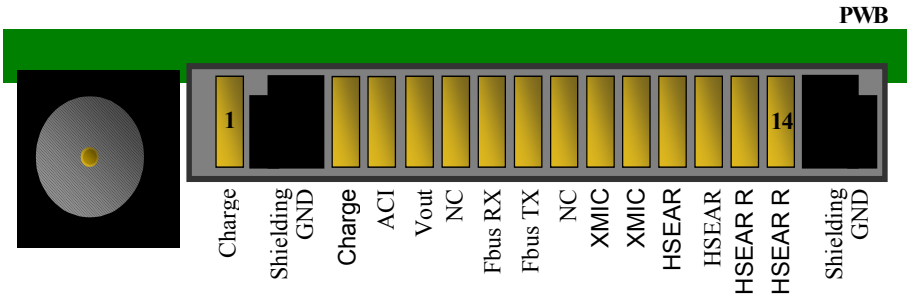
System Connector

Table 24: DC- and System Connector features

Function	Notes
Charging	Pads for 2-wire charging in cradles
Audio	- 4-wire fully differential stereo audio output - 2-wire differential microphone input
Power supply for accessories	2.78V/70mA output to accessories
FBUS	Standard FBUS

Figure 6: Charger plug socket and System Connector



External accessory regulator

An external regulator is needed for accessory power supply purposes. All ACI accessories are requiring this power supply. Regulator input is connected to main battery voltage VBAT and output is connected to System Connector VOUT pin. Regulator ON/OFF function is controlled with UPP GenI/O 0.

Table 25: Accessory Regulator Signals

Signal	Min	Nom	Max	Note
Vout	2.70V	2.78	2.86V	Imax = 150mA
GenIO(0)	1.4	1.8	1.88 0.6	High (ON) Low (OFF)

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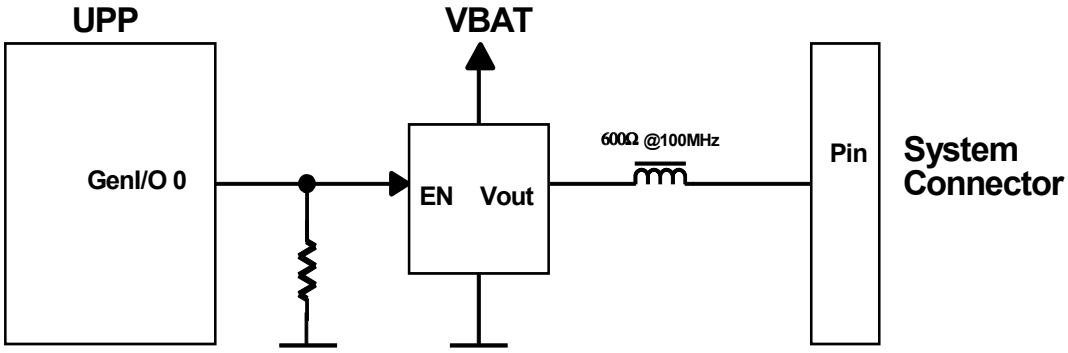
Figure 7: Accessory Power Supply Diagram



Battery

1000 mAh Li-ion battery pack BLC-2 is used in NSB-9.

Table 26: BLC-2 Characteristics

Description of phenomenon	Volts
Nominal discharge cut-off voltage	3.1V
Nominal battery voltage	3.6V
Nominal charging voltage	4.2V
Maximum charger output current	850 mA
Minimum charger output current	200 mA

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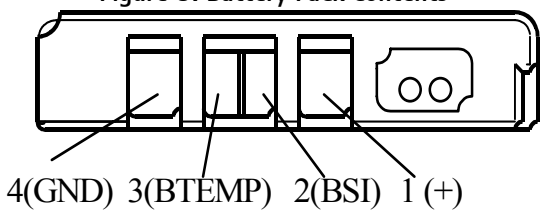
Table 27: Pin numbering of Battery Pack

Signal name	Pin number	Function
VBAT	1	Positive battery terminal
BSI	2	Battery capacity measurement (fixed resistor inside the battery pack)
BTEMP	3	Battery temperature measurement (measured by ntc resistor inside pack)
GND	4	Negative/common battery terminal

Figure 8: Battery Pack contents



The BSI fixed resistor value indicates type and default capacity of a battery. NTC-resistor BTEMP measures the battery temperature.

Temperature and capacity information are needed for charge control. These resistors are connected to BSI and BTEMP pins of battery connector. Phone has 100 kΩ pull-up resistors for these lines so that they can be read by A/D inputs in the phone.

Backup Battery

Backup battery is used in case when main battery is either removed or discharged. Backup battery is used to keep real-time clock (RTC) running for minimum of 30 minutes.

Rechargeable backup battery (capacitor type) is connected between UEM VBACK and GND. In UEM backup battery charging high limit is set to 3.2V. The cut-off limit voltage (VBUCoff-) for backup battery is 2.0V. Backup battery charging is controlled by MCU by writing into UEM register. Battery is not charged during power off.

Table 28: Back-up circuity

Parameter Test conditions	Symbol	Min	Typ	Max	Units
Back-up battery voltage	VBACK	2.43		3.3	V
Back-up battery cut-off limit	V_BU_{COFF+} V_BU_{COFF-}	2.04 1.94	2.10 2.0	2.16 2.06	V V
Charging voltage (VBAT ≥ 3.4V)	VBU	3.1	3.2	3.3	V
Charging current	I_{LIMVBU}	150		500	mA

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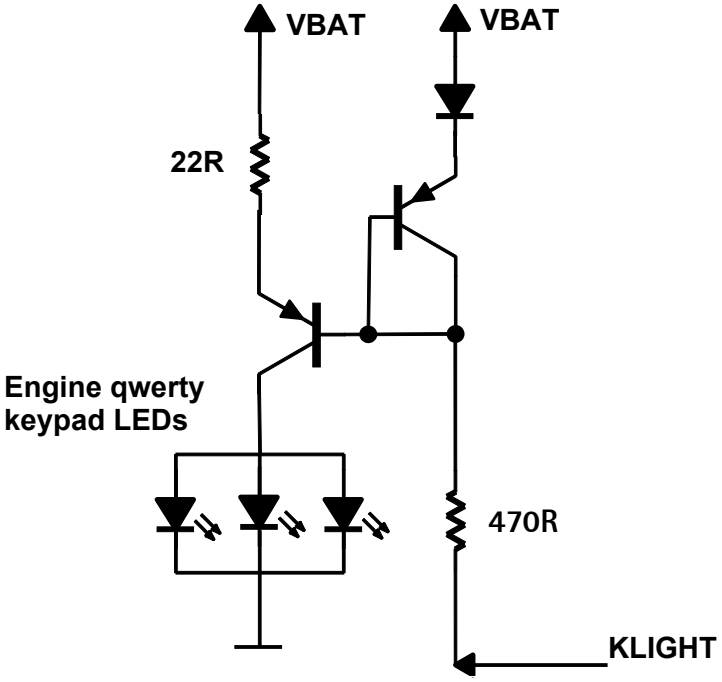
LCD & Keypad Illumination

In NSB-9 white LEDs are used for LCD and keypad illumination. For LCD illumination three LEDs are used and for keypad three in both qwerty sides and four in ITU-T keypad (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, * and #), and three in engine control keys. Engine LEDs are controlled by UEM KLIGHT and DLIGHT signals. Flip LEDs are controller by flip MCU, according to flip serial interface messages.

Figure 9: Engine qwerty keypad LED connection



Current through LEDs is controlled by transistor circuitry. External transistor driver circuitry is used as constant current source in order to prevent any change in the battery voltage to be seen as varying LED brightness.

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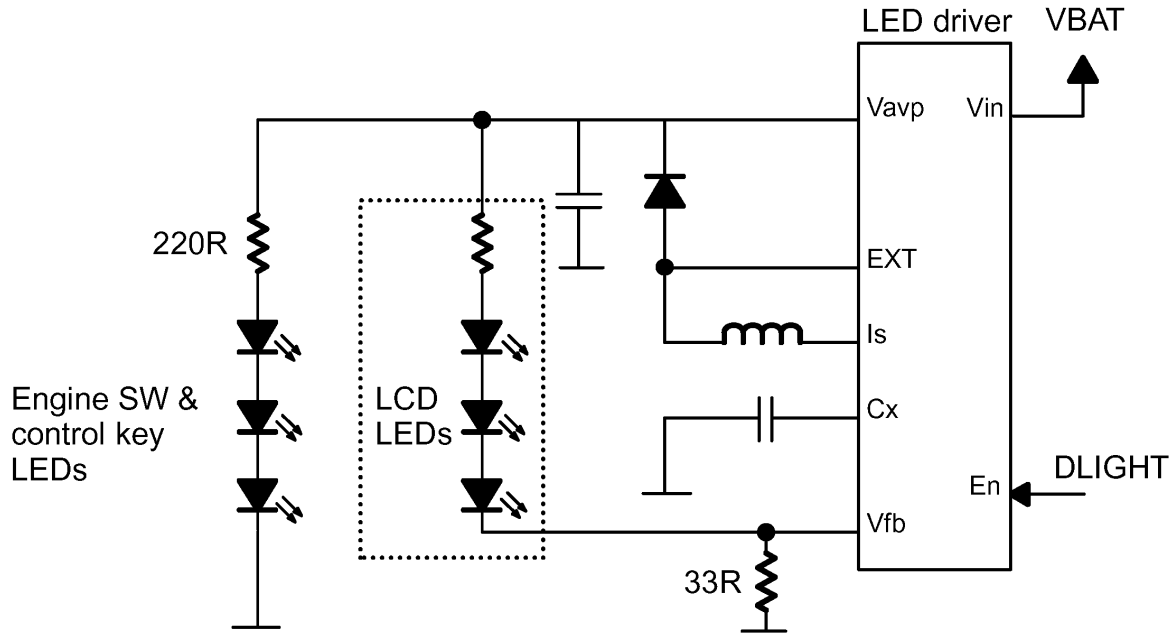
Figure 10: Engine qwerty keypad LED connection



LCD and engine SW & control keys LEDs are driven in serial mode (3 + 3 connected parallel) by a LED driver to achieve stable and bright backlightning. 33R resistor is used to define the proper current for LCD backlightning (about 16mA). The feedback signal Vfb (voltage across 33R) is used to control the current. LED driver will increase or decrease the output voltage for LEDs to keep the current stable. If current path through LCD LEDs is open, current is at its maximum and it flows through the three other LEDs

LCD

NSB-9 has 130 x 130 8bpp (bits per pixel) passive matrix colour STN display. Interface is using 9 bit data transfer. D/C bit is set during each transmitted byte.

UPP drives the CSX pin low and starts by setting the D/C-bit (data/command) to SDA. The bit is read by the display on the first rising edge of CLK. On the next falling edge of CLK the MSB data bit (D7) is set to SDA by the engine. On the next falling edge of CLK the next bit (D6) is set to SDA. This continues until all 8 bits have been transmitted.

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ACI

(Accessory Control Interface) is a point-to-point, bi-directional serial bus. ACI has three main features:

- Insertion and removal detection of an accessory device
- Identify and authenticate the connected accessory
- Data bus for accessory control

The accessories are detected by the HEADINT signal when the accessory is inserted.

Normally when no accessory is present, the 100k pull-up resistor pulls up the HEADINT signal to VFLASH1. When the accessory is inserted, the external "insertion and removal" resistor works as a voltage devider and decreases the voltage level below the threshold Vhead. Thereby the comparator output will be changed to high state causing an interrupt.

When the accessory is removed, the voltage level of HEADINT increases again to VFLASH1. This voltage level is higher than the threshold of the comparator and thereby its output will be changed to low state. This change causes an interrupt.

Those HEADINT interrupts are initiated by the accessory detection or removal sequence.

External Audio

NSB-9 is designed to support fully differential external audio accessory connection by using Pop-Port system connector. Pop-Port connector has serial data bus called ACI (Accessory Control Interface) for accessory insertion and removal detection, utilizing, identification and authentication. ACI line is also used for accessory control purposes.

Audio support with Pop-Port system connector:

- 2-wire differential mic input
- 4-wire fully differential stereo audio output (used also as an FM-radio antenna)

External Microphone Connection

The external microphone input is fully differential and lines are connected to the UEM microphone input MIC2P/N.

The UEM (MICB2) provides bias voltage. Microphone input lines are ESD protected. Creating a short circuit between the headset microphone signals (with headset button) generates the hook signal. When the accessory is not connected, the UEM resistor pulls up the HookInt signal. When the accessory is inserted and the microphone path is biased the HookInt signal decreases to 1.8V due to the microphone bias current flowing through the resistor. When the button is pressed the microphone signals are connected together, and the HookInt input will get half of micbias dc value 1.1 V. This change in DC level will

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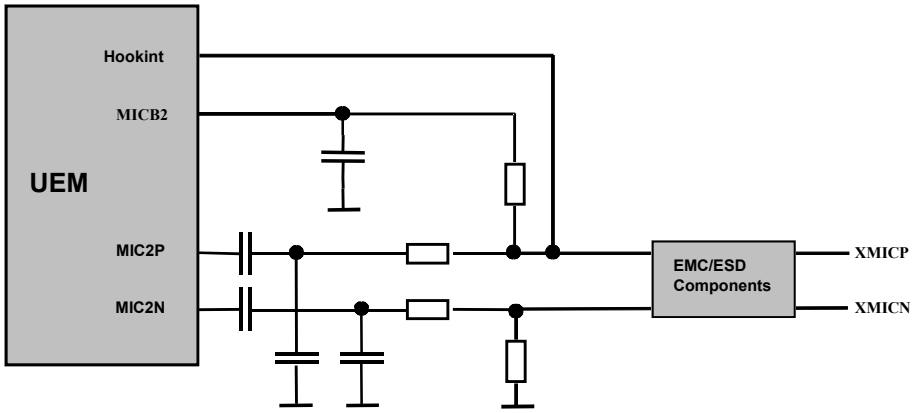
cause the HookInt comparator output to change state, in this case from 0 to 1. The button can be used for answering incoming calls and then ending them. The button can be used for initiating outgoing calls, if voice tags are saved for dialing.

Figure 11: External microphone connection



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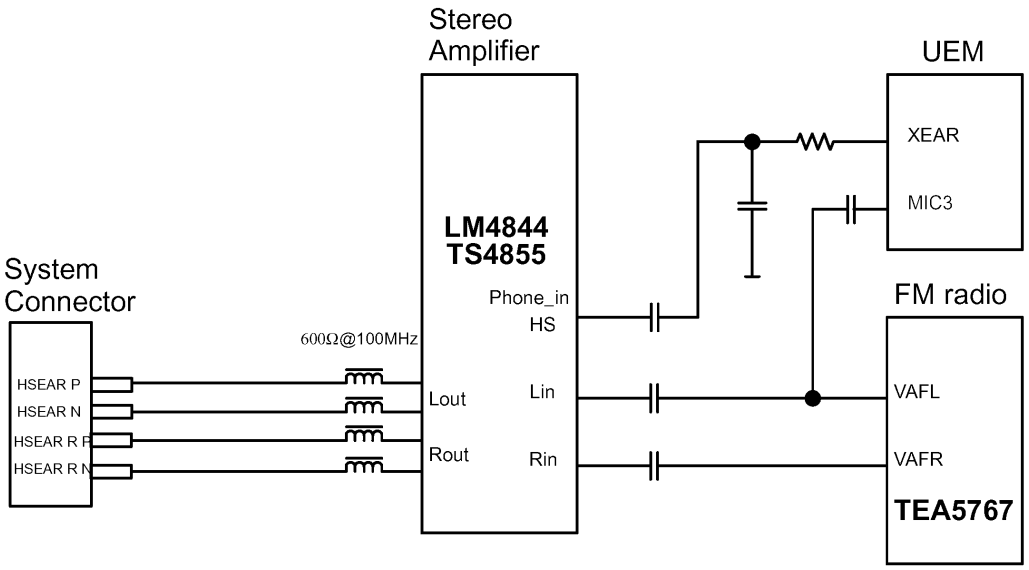
External Earphone Connections

Figure 12: System connector

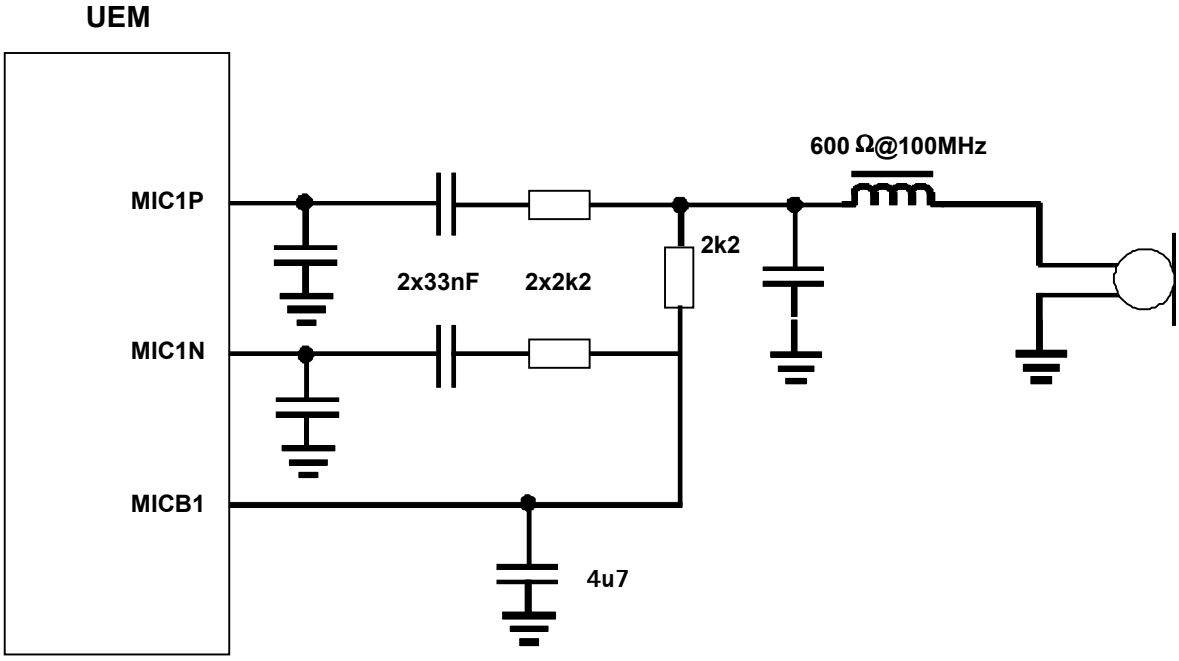


Internal Audio

Internal Microphone

The internal microphone module and holder is mounted into the B-cover. Microphone is omni directional. The internal microphone is connected to the UEM microphone input MIC1P/N. The microphone input is asymmetric and microphone bias is provided by the UEM MIC1B. The microphone input on the UEM is ESD protected. Spring contacts are used to connect the microphone contacts to the main PWB.

Figure 13: Internal microphone connections



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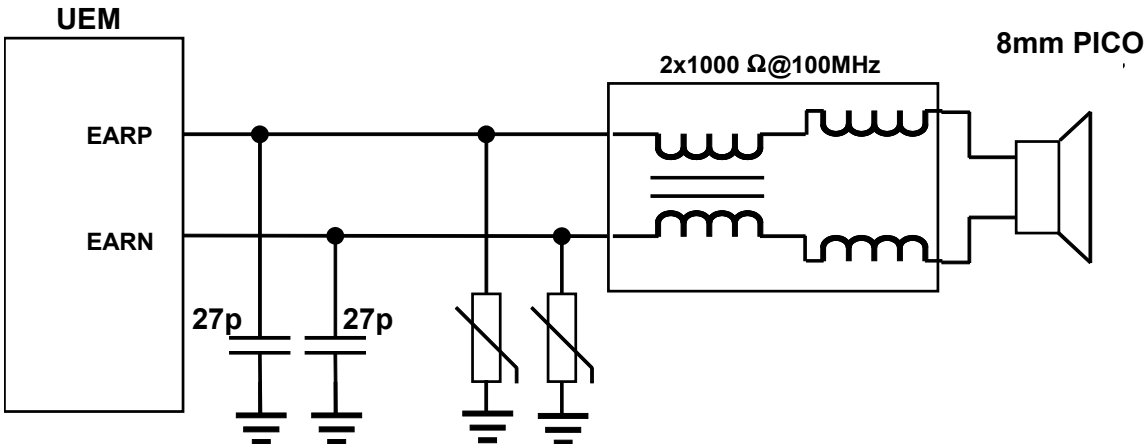
Internal Speaker

The internal earpiece is mounted into the LCD metal frame. The earpiece is a dynamic earpiece with a 32 ohm impedance. The earpiece is low impedance one since the sound pressure is to be generated using current and not voltage as the supply voltage is restricted to 2.7V. The earpiece is driven directly by the UEM. The earpiece driver in UEM is a bridge amplifier.

Figure 14: Internal speaker connections



Integrated Hands Free

Integrated Handsfree (IHF) makes it possible to keep the phone for example on desk and keep both hands free. When IHF mode is activated, internal microphone is used as in HP-mode and IHF speaker is used instead of earpiece.

The FM-radio can be listened from the IHF speaker as well, if a headset is connected (FM-radio antenna).

The stereo audio amplifier supports four inputs and three outputs. It is capable of delivering 340mW of continuous averahe power into a mono 8Ohm bridged-tied load and 25mW per channel of continuous average power into stereo 32Ohm loads (when using 3V supply voltage). Stereo signal from FM-radio is connected to Rin and Lin inputs, and XEAR signal from UEM is connected to PhoneInHS input of stereo audio amplifier. Phone IHF line includes discrete RC high-pass filtering in order to cut off low frequencies from IHF speaker. SPKROut lines are connected to IHF speaker. PhoneInIHF to SPKROut path has fixed 12dB gain.

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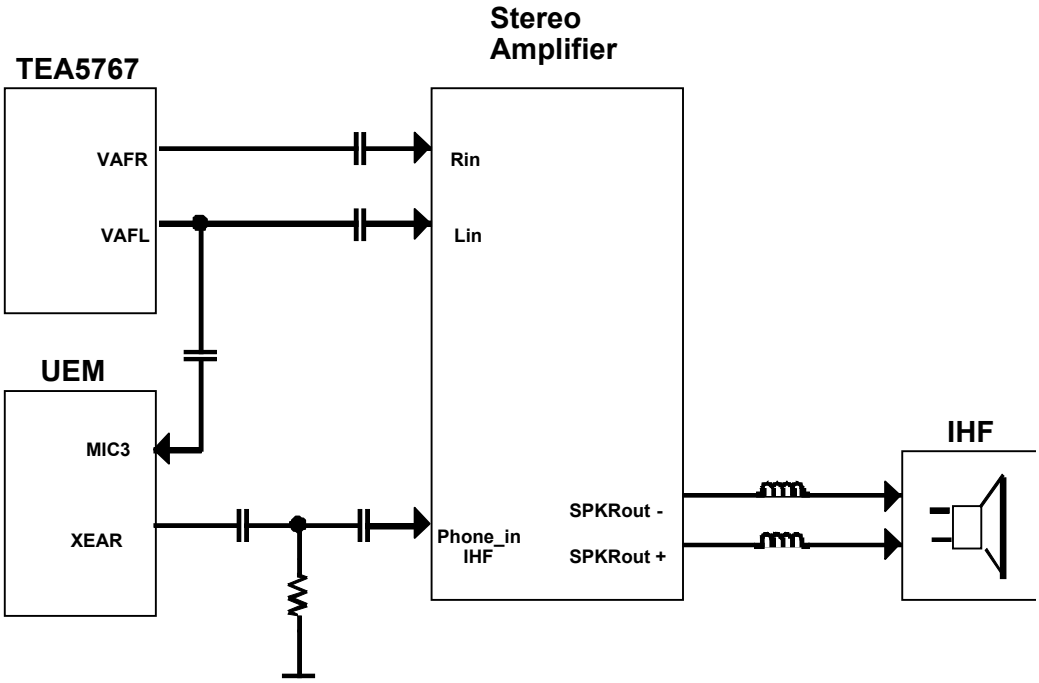
Figure 15: IHF connections



Memory Block

For the MCU UPP includes ROM, 2 kbytes, that is used mainly for boot code of MCU. To speed up the MCU operation small 64 byte cache is also integrated as a part of the MCU memory interface. For program memory 8Mbit (512k x 16bit) PDRAM is integrated into UPP, and 8Mbit external SRAM is in separate COMBO MEMORY chip. RAM block can also be used as data memory and it is byte addressable. RAM is mainly for MCU purposes but also DSP has also access to it if needed.

MCU code is stored into external flash memory, which is in a combo memory chip. The size of the flash is 128Mbit (8M x 16bit). The NSB-9 baseband supports a burst mode flash with multiplexed address/data bus. Access to the flash memory is performed as 16-bit access. The flash has Read While Write capabilities which makes the emulation of EEPROM within the flash easy.

Security

The phone flash program and IMEI code are software protected using an external security device that is connected between the phone and a PC.

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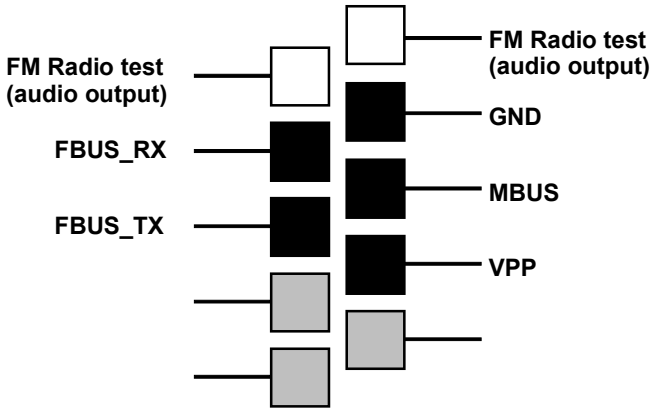
Production / After Sales Interface

Test pads are placed on engine PWB bottom side for service and production trouble shooting purposes.

The standard 5 pin test pattern is shown in figure below. NSB-9 has two pins for FM-radio testing. The pins are connected in parallel with two system connector audio output lines (HSEAR P and HSEAR R N). The FM radio can be tested between those lines.

Figure 16: Flash and FM-radio test connection



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